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1. Ku-Band Chipset Solution

1.1 Ku-Band 0.5W 4-Channel T/R Chipset Solution

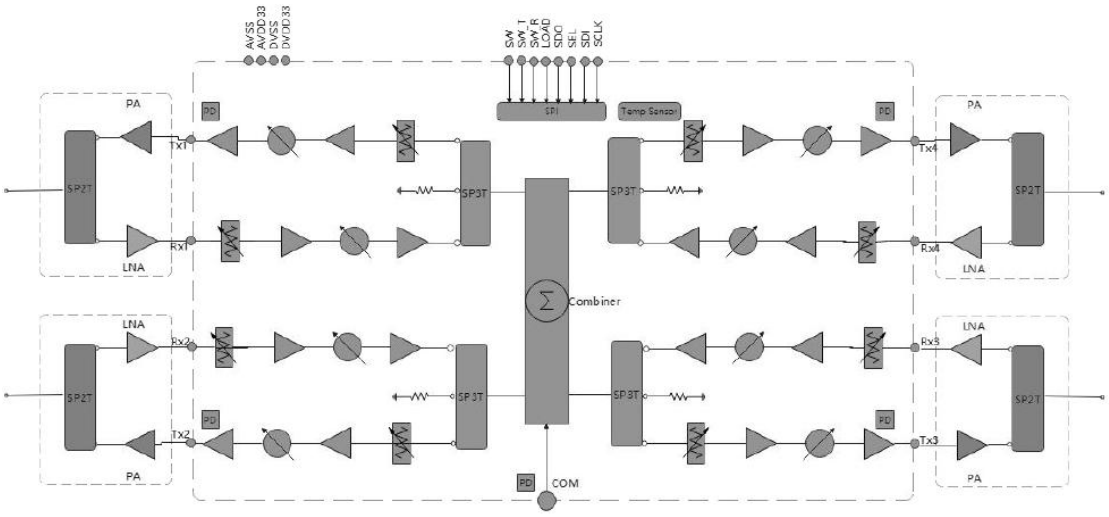

Figure 1 Ku-Band 0.5 W T/R Chipset System Architecture Diagram

To meet the application requirements of Ku-band four-channel T/R modules, a T/R chipset solution consisting of the four-channel silicon-based amplitude-phase control multi-function chip XSC-6520, XTR-1418-30A1 GaAs 0.5 W T/R chip and XPM-5V1A power modulation chip is proposed.

The XSC-6520 four-channel silicon-based amplitude-phase control multi-function chip contains four transmit channels and four receive channels. The receive channels support independent 6-bit phase tuning and 6-bit amplitude tuning, while the transmit channels support independent 6-bit phase tuning and 5-bit amplitude tuning. Each transmit channel is equipped with a power detection function, and an on-chip temperature sensor is integrated inside the chip. The output power and chip temperature can be read back via SPI. Meanwhile, the chip automatically performs gain compensation according to the detected temperature. In transmit mode, the RF input signal passes through a power divider and feeds into the four transmit channels. In receive mode, the received RF signals go through the four receive channels and are combined into a single path via a power combiner for output at the common port. TX denotes the transmit output port, RX denotes the receive input port, COM denotes the common RF port, Temp Sensor stands for temperature detection, and PD stands for power detection.

The XTR-1418-30A1 GaAs 0.5 W T/R chip integrates a power amplifier, a limiter low-noise amplifier and a RF switch.

The XPM-5V1A power modulation chip is a high-current power modulator fabricated using silicon process technology. It can supply multi-channel power drive for T/R circuits, including one set of T/R channel power drive circuits and one set of T/R switch signal output circuits.

1.1.1. Chip Design Solution

1.1.1.1 Silicon-Based 4-Channel Amplitude-Phase Multi-Function Chip

- Operating Frequency: 12 GHz~18.5 GHz
- Rx Gain: ⩾2 dB

  Note: including 1-to-4 power division loss, adjustable up to 7.5 dB
- Tx Gain: ⩾10 dB

  Note: including 1-to-4 power division loss, 13 dB @ Pin = 2 dBm
- Rx Input P-1: 0 dBm
- Tx Output P-1: 15 dBm
- Phase Shift Resolution: 6 bits
- Phase Shift Step: 5.625°
- Phase Shift Error (RMS): 3°
- Phase Shift Amplitude Variation: ±1 dB
- RX Attenuation Range: 0~31.5dB/6bits
- RX Attenuation Step: 0.5dB
- RX Attenuation Error (RMS): 0.25dB
- RX Attenuation Phase Variation: 8°
- TX Attenuation Range: 0~15.5dB/6bits
- TX Attenuation Step: 0.5dB
- TX Attenuation Error (RMS): 0.25dB
- TX Attenuation Phase Variation: 8°
- Operating Voltage: Digital/Analog, 3.3 V; RF, 3.3 V or 1.8 V (selectable)
- RX Quiescent Current: 68 mA/Chanel
- Tx Dynamic Current: 140 mA /Chanel
- Chip Dimensions: 3.5 mm × 6.5 mm × 0.2 mm

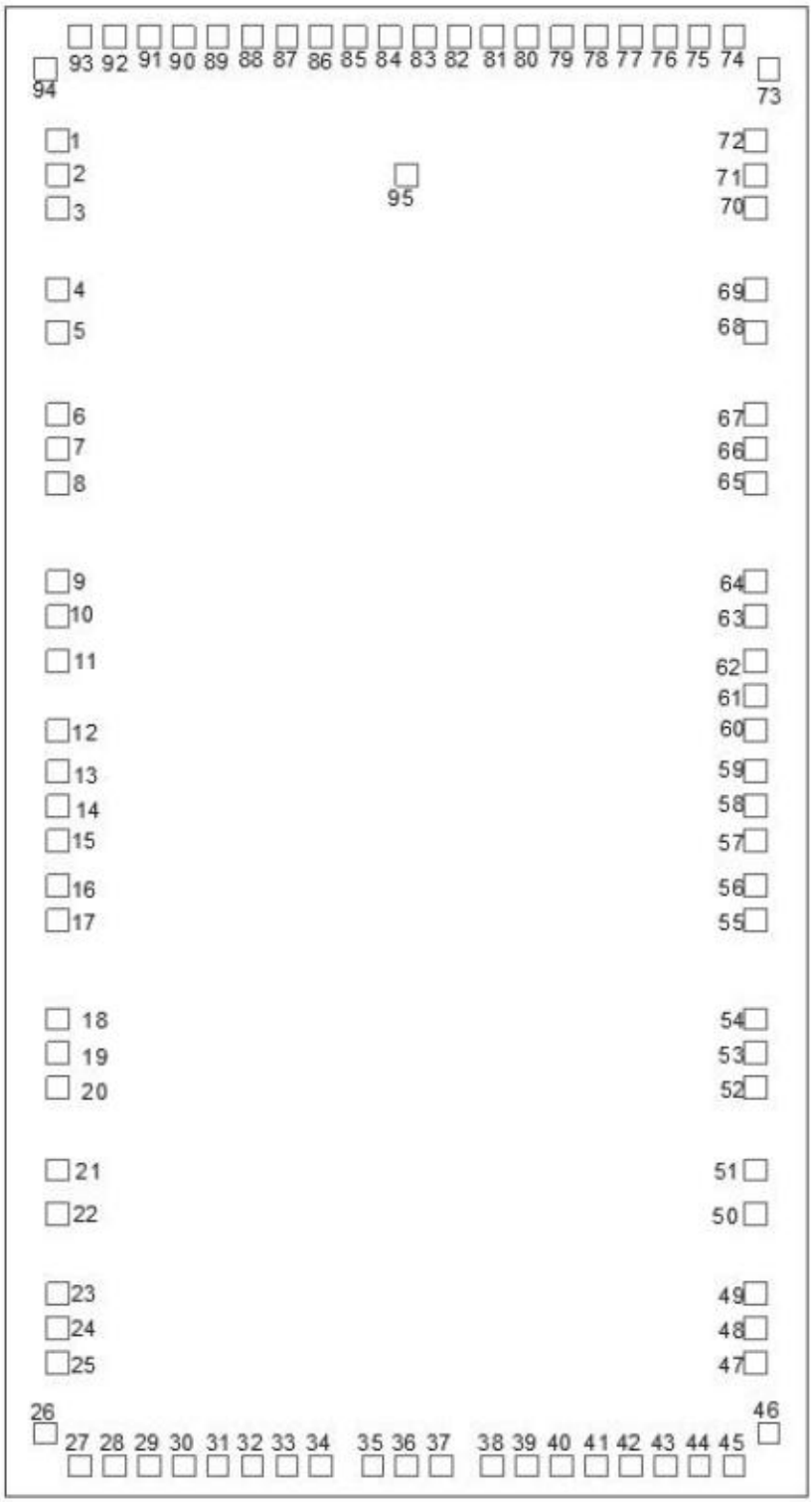

Figure 2 Pad Layout of XSC-6520

Table 1 Pad Definition of XSC-6520

PAD				Description	Notes
No.	Name	Size (um)	Type		
1	TX1_G1	100x100	GND	RF GND	
2	TX1_S	100x100	OUTPUT	RF Output of CH1	
3	TX1_G2	100x100	GND	RF GND	
4	TX1_EN	100x100	OUTPUT	TX Enable, CH1	
5	AVSS	100x100	GND	RF GND	
6	RX1_G1	100x100	GND	RF GND	
7	RX1_S	100x100	INPUT	RF Input, CH1	
8	RX1_G2	100x100	GND	RF GND	
9	RX1_EN	100x100	OUTPUT	RX Enable, CH1	
10	LNA1_VG	100x100	OUTPUT	External LNA Gate Bias Voltage for CH1	
11	AVSS	100x100	GND	RF GND	
12	AVSS	100x100	GND	RF GND	
13	AVDD33	100x100	POWER	Analog 3.3V Supply	
14	LDO_SW	100x100	INPUT	LDO Select Switch	
15	AVSS	100x100	GND	RF GND	
16	LNA2_VG	100x100	OUTPUT	External LNA Gate Bias Voltage for CH2	
17	RX2_EN	100x100	OUTPUT	RX Enable, CH2	
18	RX2_G2	100x100	GND	RF GND	
19	RX2_S	100x100	INPUT	RF Input, CH2	
20	RX2_G1	100x100	GND	RF GND	
21	AVSS	100x100	GND	RF GND	

22	TX2_EN	100x100	OUTPUTT	TX Enable, CH2	

23	TX2_G2	100x100	GND	RF GND	
24	TX2_S	100x100	OUTPUT	RF Output, CH2	
25	TX2_G1	100x100	GND	RF GND	
26	AVDD33_RF	100x100	POWER	RF 3.3V Supply	
27	AVDD18_CH2	100x100	POWER	1.8V Supply, CH2	
28	AVSS	100x100	GND	RF GND	
29	SPI_MODE_SEL	100x100	INPUT	SPI Mode Selection: Low level for 4-wire mode, high level for 3-wire mode	
30	SPI_SEL3	100x100	INPUT	Protocol Selection	GND
31	SPI_SEL2	100x100	INPUT	Protocol Selection	GND
32	SPI_SEL1	100x100	INPUT	Protocol Selection	GND
33	TX_EN	100x100	OUTPUT	TX Enable Flag	
34	RX_EN	100x100	OUTPUT	RX Enable Flag	
35	RF_COM_G1	100x100	GND	RF GND	
36	RF_COM_S	100x100	IN/OUTPUT	Common RF Port	
37	RF_COM_G2	100x100	GND	RF GND	
38	AVSS	100x100	GND	RF GND	
39	AVDD33	100x100	POWER	Analog 3.3V Supply	
40	-	100x100	-	-	
41	ID4	100x100	INPUT	ID Bit	Default: Low
42	ID5	100x100	INPUT	ID Bit	Default: Low
43	ID6	100x100	INPUT	ID Bit	Default: Low
44	AVSS	100x100	GND	RF GND	
45	AVDD18_CH3	100x100	POWER	1.8V Supply, CH3	

46	AVDD33_RF	100x100	POWER	RF 3.3V Supply	

47	TX3_G1	100x100	GND	RF GND	
48	TX3_S	100x100	OUTPUT	RF Output, CH3	
49	TX3_G2	100x100	GND	RF GND	
50	TX3_EN	100x100	OUTPUT	TX Enable, CH3	
51	AVSS	100x100	GND	RF GND	
52	RX3_G1	100x100	GND	RF GND	
53	RX3_S	100x100	INPUT	RF Input, CH3	
54	RX3_G2	100x100	GND	RF GND	
55	RX3_EN	100x100	OUTPUT	RX Enable, CH3	
56	LNA3_VG	100x100	OUTPUT	External LNA Gate Bias Voltage for CH3	
57	AVSS	100x100	GND	RF GND	
58	-	100x100	-	-	
59	AVDD33	100x100	POWER	Analog 3.3V Supply	
60	AVSS	100x100	GND	RF GND	
61	-	100x100	-	-	
62	AVSS	100x100	GND	RF GND	
63	LNA4_VG	100x100	OUTPUT	External LNA Gate Bias Voltage for CH4	
64	RX4_EN	100x100	OUTPUT	RX Enable, CH2	
65	RX4_G2	100x100	GND	RF GND	
66	RX4_S	100x100	INPUT	RF Input, CH4	
67	RX4_G1	100x100	GND	RF GND	
68	AVSS	100x100	GND	RF GND	

69	TX4_EN	100x100	OUTPUT	TX Enable, CH3	
70	TX4_G2	100x100	GND	RF GND	
71	TX4_S	100x100	OUTPUT	RF Output, CH4	
72	TX4_G1	100x100	GND	RF GND	
73	AVDD33_RF	100x100	POWER	RF 3.3V Supply	
74	AVDD18_CH4	100x100	POWER	1.8V Supply, CH4	
75	AVSS	100x100	GND	RF GND	
76	ID0	100x100	INPUT	ID Bit	Default High
77	ID1	100x100	INPUT	ID Bit	Default Low
78	ID2	100x100	INPUT	ID Bit	Default Low
79	ID3	100x100	INPUT	ID Bit	Default Low
80	SW_R	100x100	INPUT	T/R Switch, SW_R	Default Low
81	SW_T	100x100	INPUT	T/R Switch, SW_T	Default Low
82	SW	100x100	INPUT	T/R Switch, SW	Default Low
83	DVSS	100x100	GND	Digital GND	
84	DVDD33	100x100	POWER	Digital 3.3V Supply	
85	RESET	100x100	INPUT	Reset Signal	
86	SDO	100x100	OUTPUT	Serial Data Output	
87	SCLK	100x100	INPUT	Serial Clock	
88	SDI	100x100	IN/OUTPUT	Serial data: auto I/O in 3-wire SPI mode, input only in 4-wire SPI mode	
89	SYNC	100x100	INPUT	Chip Select signal, active low	
90	LOAD	100x100	INPUT	Latch signal, rising edge triggered	
91	-	100x100	-	-	

92	AVSS	100x100	GND	RF GND	
93	AVDD18_CH1	100x100	POWER	1.8V Supply, CH1	
94	AVDD33_RF	100x100	POWER	RF 3.3V Supply	
95	VDDQ	200x200	POWER	eFuse 2.5V Supply	

1.1.1.2 XTR-1418-30A1，GaAs Multifunction T/R Chip

- Operating Frequency: 14 GHz~18 GHz
- TX Power Gain: 21 dB
- Saturated Output Power: 28.1 dBm
- PAE: 34%
- RX Channel Gain: 25 dB
- Rx Input P-1: -20 dBm
- Noise Figure: 3.2 dB
- RX Quiescent Power Consumption: +3.3 V / 20 mA (Typical)
- Chip Size: 2.80mm×2.40mm×0.10mm
- Mirror Version Available

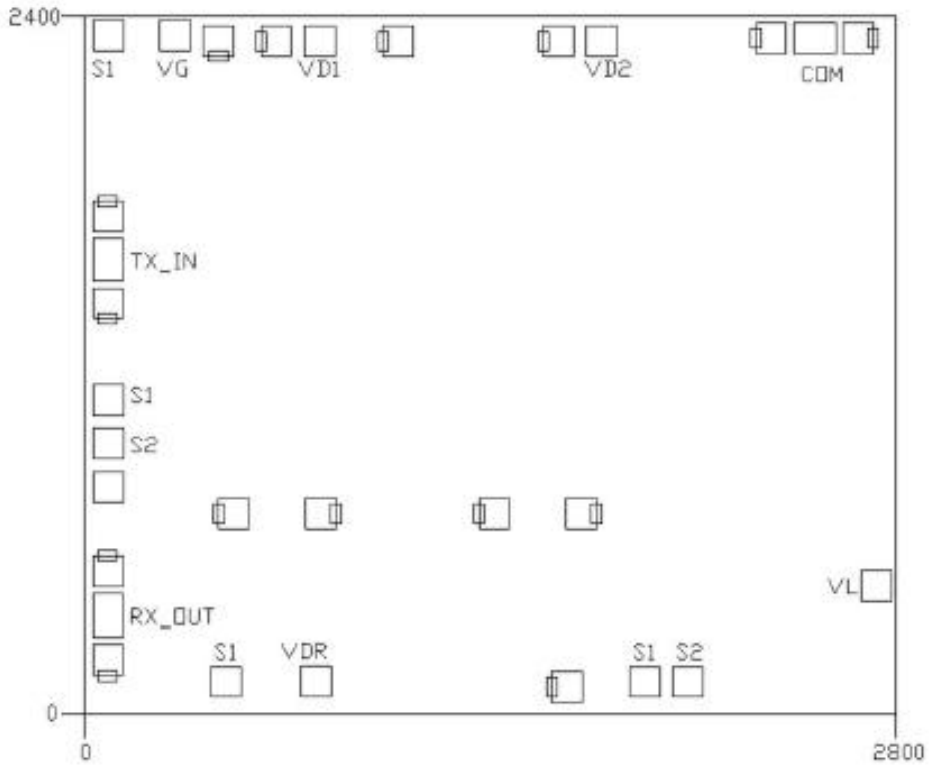

Figure 3 GaAs Multifunction T/R Chip Pad Layout

Table 2 GaAs Multifunction T/R Chip Pad Assignments

Pad Designation	Description
VG	TX Gate Vbias, -1V
VD1,2	TX Drain Vdd, 3.3V
COM	Common RF Port
VL	Limiter Ctrl Voltage, -5V
S1，2	SW Ctrl Voltage, 5V/0V
VDR	RX Drain Vdd, 5V
RX_OUT	RX RF Out Port
TX_IN	TX RF In Port

1.1.1.3 XPM-5V1A Power Modulating IC

The XPM-5V1A power modulation chip is a high-current power modulator fabricated using silicon process technology. This device is capable of providing multi-channel TR module power supply driving, consisting of one set of TR channel power drive circuits and one set of TR switching signal output circuits. The PMOS power transistor drive circuit for the transmit (T) channel is designed to control the 5 V power rail of the GaAs power amplifier. It integrates negative supply undervoltage protection, enable on/off control, rapid drain discharge, and over-pulse-width protection functions. The gate bias voltage VG of the GaAs power amplifier is adjustable via the 4-bit control bus D<3:0>, and its output range can be switched through the RGS<1:0> ports. Four voltage ranges are available: -0.6 V ~ -1.35 V, -1.25 V ~ -2.0 V, -1.9 V ~ -2.65 V, -2.55 V ~ -3.3 V. The voltage step resolution is 50 mV.

The chip system mainly consists of a logic control module, positive and negative voltage undervoltage protection circuits, high-voltage driver modules, low-voltage modulation circuits, an SW/SOC delay control module and a selective output circuit. The system block diagram is shown in the figure below:

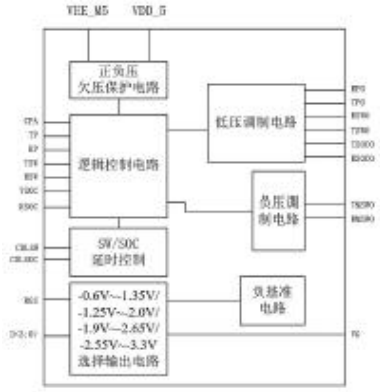

Figure 4 System Block Diagram of XPM-5V1A

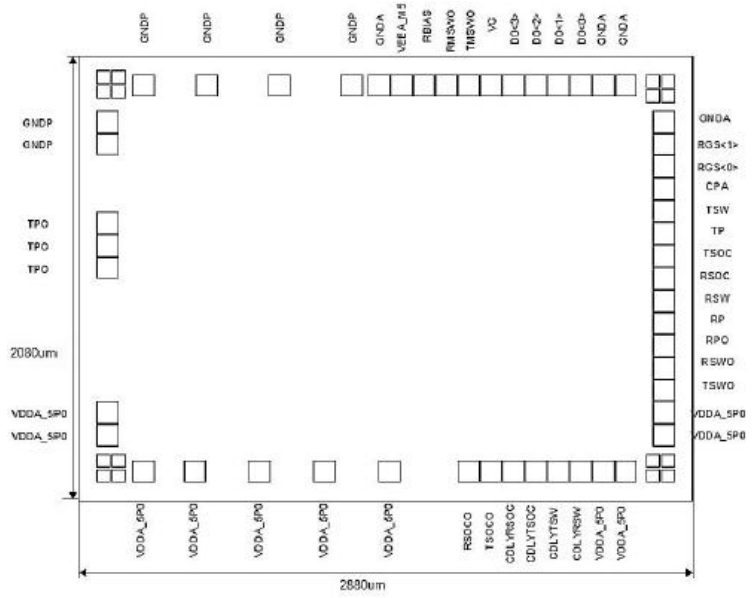

Figure 5 Pad & Outline Dimensions of XPM-5V1A

Table 3 Pad Assignments for XPM-5V1A

Pad	Function Descriptin	Note
CPA	OPW Protection Setup	
CDLSW	SWTR Delay Config	
CDLSOC	SOCTR Delay Config	
RGS	VG Range Select	
VG	GaN VG Output	
D<3:0>	GaN VG Adjust Bits	
TP	Tx Power Ctrl	

TSW	Tx SW Ctrl	
TSOC	SOC Tx Ctrl	
RP	Rx Power Ctrl	
RSW	Rx SW Ctrl	
RSOC	SOC Rx Ctrl	
TPO	Tx Power	
TSWO	Tx SW	
RPO	Rx Power	
RSWO	Rx SW	
TSOCO	SOC Tx Ctrl Output	
RSOCO	SOC Rx Ctrl Output	
TMSWO	Negative Voltage Tx Switch	
RMSWO	Negtive Voltage Rx Switch	
VEE_M5	-5V	
VDD_5	5V	
GND	Ground	
PGND	Power Ground	

1.1.2. Solution Summary

The solution consists of a four-channel silicon-based multi-functional chip and four GaAs transceiver multi-functional chips. It will use +5V、+3.3V、-5V、+1.8V(optional) power supply voltage rails. The overall link budget specifications of the T/R chipset are shown in Table 4 below:

Table 4 Specifications of Ku-Band 0.5W 4-Channel T/R Chipset

TX or RX	Parameter	Typical Value	Note
TX	Tx Gain	22dB	Adjustable Gain 30dB
	Tx Output Power	28.1dBm	
	Tx Power Consumption	1.914W	

	Tx Efficiency	31.2%	
	Atten. Bits / Step	5bits/0.5dB	
	Atten. Accuracy	≤0.5dB	
	Phase Shift Bits / Step	6bits/5.625°	
	Phase Shift Accuracy（RMS）	≤2.5°	
	Phase Shift Spurious AM	±1dB	
RX	Rx Gain	26dB	Single channel, including power divider insertion loss
	Noise figure	≤3.2dB	Single channel
	Rx Input P-1dB	≥-20dBm	
	Rx Power Consumption	0.19W(1.8V supply) 0.29W(3.3V supply)	Single Channel
	Atten. Bits / Step	6bits/0.5dB	
	Atten. Accuracy	≤0.4dB	

	Phase Shift Bits / Step	6bits/5.625°	
	Phase Shift Accuracy（RMS）	≤3°	
	Phase Shift Spurious AM	±1dB	

1.2 Ku-Band 1W 4-Channel T/R Chipset Solution

System breakdown of Ku-Band 1W T/R Chipset, see Figure 1 for details.

1. 2. 1 Chip Design Solution

1.2.1.1 Silicon-Based 4-Channel Amplitude-Phase Multi-Function Chip

Refer to 1.1.1.1.

1.2.1.2 GaAs Multifunction T/R Chip

- Operating Frequency: 14 GHz~18 GHz

- TX Power Gain: ⩾24dB
- Saturated Output Power: ⩾31dBm
- PAE: ⩾34%
- Tx Supply: VD +5V, VG -0.5V
- RX Channel Gain: ⩾24dB
- Rx Output P-1: ⩾-2 dBm
- Noise Figure: ⩽2.7 dB
- RX Power Consumption: +5V/16mA
- Input/Output VSWR: 2.0/1.5
- Switch Ctrl: 0V/+5V
- Chip Size: 2.80mm×2.60mm×0.10mm

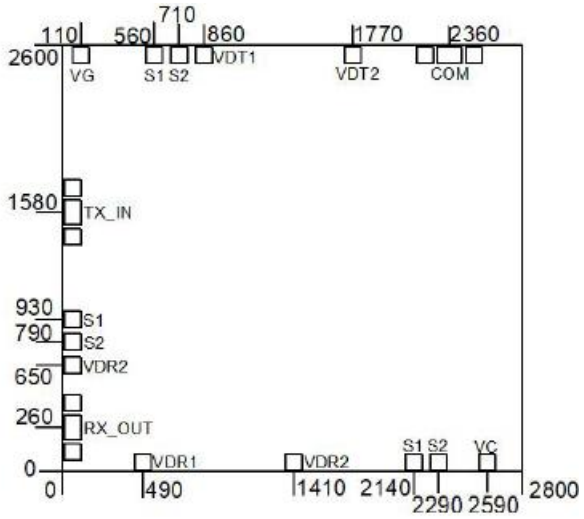

Figure 6 Pad Drawing of GaAs T/R Multi-Function Chip

1.2.1.3 XPM-5V1A Power Modulating IC

Refer to 1.1.1.3

1. 2. 2 Solution Summary

The solution consists of a four-channel silicon-based multi-functional chip and four GaAs transceiver multi-functional chips. It will use +5V、+3.3V、-5V、+1.8V(optional) power supply voltage rails. The overall link budget specifications of the T/R chipset are shown in Table 5 below:

Table 5 Specifications of Ku-Band 0.5W 4-Channel T/R Chipset

TX or RX	Parameter	Typical Value	Note

TX	Tx Gain	27dB	Adjustable Gain 35dB
	Tx Output Power	31dBm	
	Tx Power Consumption	3.7W	
	Tx Efficiency	34%	
	Atten. Bits / Step	5bits/0.5dB	
	Atten. Accuracy	≤0.5dB	
	Phase Shift Bits / Step	6bits/5.625°	
	Phase Shift Accuracy（RMS）	≤23°	
	Phase Shift Spurious AM	±1dB	
RX	Rx Gain	24dB	Single channel, including power divider insertion loss
	Noise figure	≤3dB	Single channel
	Rx Input P-1dB	≥-26dBm	
	Rx Power Consumption	0.2W(1.8V supply) 0.3W(3.3V supply)	Single Channel
	Atten. Bits / Step	6bits/0.5dB	
	Atten. Accuracy	≤0.4dB	
	phase shifter	6bits/5.625°	
	Phase Shift Accuracy（RMS）	≤3°	
	Phase Shift Spurious AM	±1dB	

1.3 Ku-Band 2W 4-Channel T/R Chipset Solution

System breakdown of Ku-Band 2W T/R Chipset, see Figure 1 for details.

1.3.1 Chip Design Solution

1.3.1.1 Silicon-Based 4-Channel Amplitude-Phase Multi-Function Chip

Refer to 1.1.1.1.

1.3.1.2 XTR-1418-33 Multifunction T/R Chip

- Operating Frequency: 14 GHz~18 GHz
- TX Power Gain: ⩾24.5dB
- Saturated Output Power: ⩾33dBm
- PAE: ⩾31.8%
- Tx Supply: VD +5V, VG -0.5V
- Dynamic Current: 1.2A(Typ.) 1.3A(Max.)
- RX Channel Gain: ⩾23.5dB
- Rx Output P-1: ⩾4dBm
- Noise Figure: ⩽3.2 dB
- RX Power Consumption: +5V/22mA
- RF Switch Switching Time: 20ns
- Switch Ctrl: 0V/+5V
- Chip Size: 3.4mm×2.85mm×0.10mm

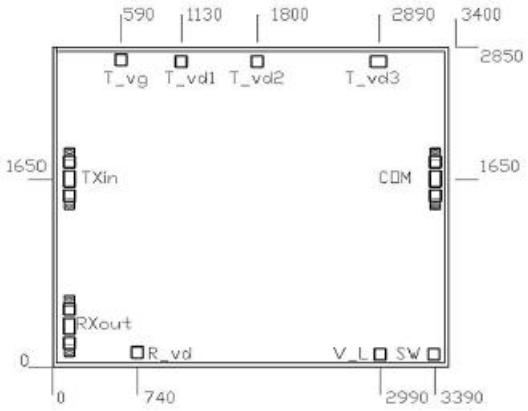

Figure 7 Pad Drawing of XTR-1418-33

Table 6 Pad Assignments for XTR-1418-33

Pad Designation	Function Description
TXin	PA Input
Rxout	LNA Output
R_vd	Rx Drain Supply

V_L	Limiter Ctrl Level
SW	Switch Ctrl Voltage
COM	Common RF Port
T_vd3	PA Drain Supply
T_vd2	PA Drain Supply
T_vd1	PA Drain Supply
T_vg	PA Gate Supply

1.3.1.3 XPM-5V1A Power Modulating IC

Refer to 1.1.1.3

1.3.2 Solution Summary

The solution consists of a four-channel silicon-based multi-functional chip and four GaAs transceiver multi-functional chips. It will use +5V、+3.3V、-5V、+1.8V(optional) power supply voltage rails. The overall link budget specifications of the T/R chipset are shown in Table 5 below:

Table 7 Specifications of Ku-Band 2W 4-Channel T/R Chipset

TX or RX	Parameter	Typical Value	Note
TX	Tx Gain	35.5dB	Adjustable Gain 30dB
	Tx Output Power	33dBm	
	Tx Power Consumption	6.5W	
	Tx Efficiency	30.7%	
	Atten. Bits / Step	5bits/0.5dB	
	Atten. Accuracy	≤0.5dB	
	Phase Shift Bits / Step	6bits/5.625°	
	Phase Shift Accuracy（RMS）	≤3°	
	Phase Shift Spurious AM	±1dB	
RX	Rx Gain	25.5dB	Single channel, including power divider insertion loss
	Noise figure	≤3.4dB	Single channel
	Rx Input P-1dB	≥-24dBm	

	Rx Power Consumption	0.23W	Single Channel
	Atten. Bits / Step	6bits/0.5dB	
	Atten. Accuracy	⩽0.4dB	
	phase shifter	6bits/5.625°	
	Phase Shift Accuracy（RMS）	⩽3°	
	Phase Shift Spurious AM	±1dB	

1.4 Ku-Band 2.5W 4-Channel T/R Chipset Solution

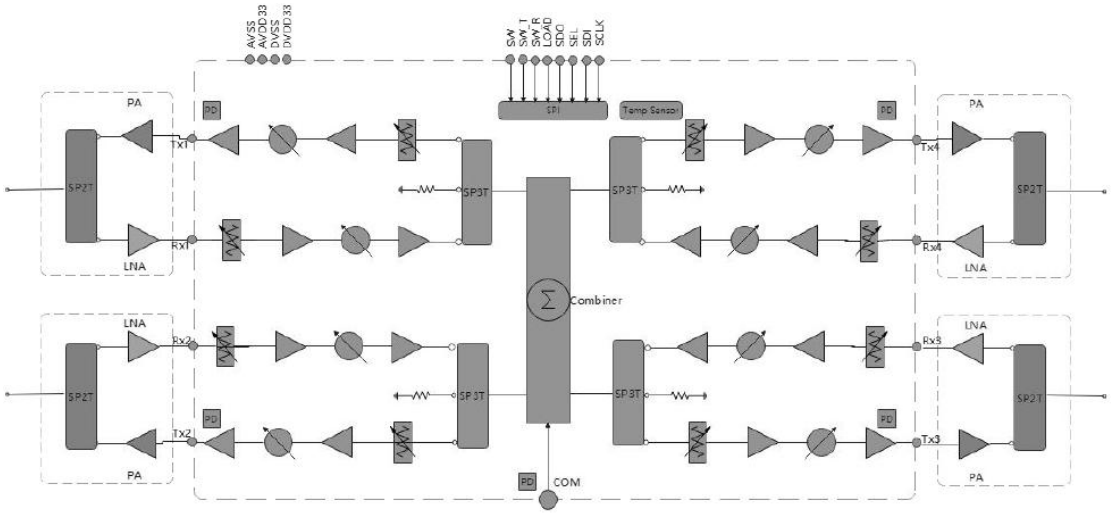

Figure 8 Ku-Band 2.5 W T/R Chipset System Architecture Diagram

1.4.1 Chip Design Solution

1.4.1.1 Silicon-Based 4-Channel Amplitude-Phase Multi-Function Chip

Refer to 1.1.1.1.

1.4.1.2 XTR-1418A(M) PA Switch Chip

Operating Frequency: 14 GHz~18 GHz

- TX Power Gain: ⩾23dB
- Saturated Output Power: ⩾33.5dBm
- PAE: ⩾37%
- Power Consumption: ⩽28V/350mA

- Rx Switch Insertion Loss: ≤0.9dB
- Switching Time: 20ns
- Input Return Loss: -15dB
- Output Return Loss: -15dB
- Chip Size: 3.2mm×1.45mm×0.10mm

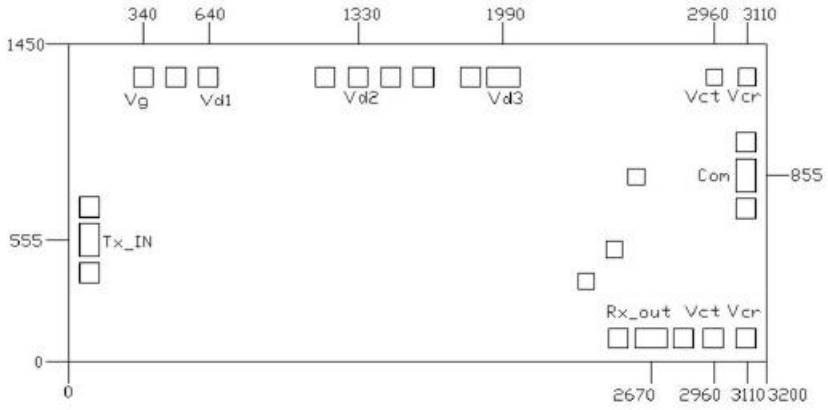

Figure 9 Pad Drawing of XTR-1418A(M)

Table 8 Pad Assignments for XTR-1418(M)

Pad Designation	Function Description	Note
Tx_IN	Tx RF Input Port	
Rx_out	Rx RF Output Port	
Vct	Switch Ctrl Voltage Port 1 (Vct Pad, 1-of-2)	SW1=0V,SW2=-28V, Tx Channel Active; SW1=-28V,SW2=0V, Rx Channel Active;
Vcr	Switch Ctrl Voltage Port 2 (Vct Pad, 1-of-2)	
COM	RF Common Port	
Vd1,2,3	Tx PA Drain Supply	28V
Vg	Tx PA Gate Supply	

1.4.1.3 XLT-1218A(M) Limiter-LNA Chip

- Operating Frequency: 12 GHz~18.5 GHz
- Gain: 26dB
- Noise Figure: ≦3.2 dB
- Input P-1: ≥-22dBm
- Power Handling: 5W
- Input Return Loss: -15dB
- Output Return Loss: -15dB

- Power Consumption: 5V/28mA
- Chip Size: 2.3mm×1.2mm

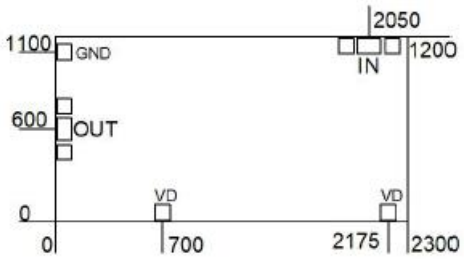

Figure 10 Pad Drawing of XLT-1218(M)

Table 9 Pad Assignments for XLT-1218(M)

Pad Designation	Function Description
IN	RF input
OUT	RF Output
VD	Drain Supply
GND	Gnd PAD

1.4.2 Solution Summary

The solution consists of a four-channel silicon-based multi-functional chip, PA switch chip and limiter-LNA chip. It will use +28V、-28V、+5V、-5V、+3.3V、+1.8V(optional) power supply voltage rails. The overall link budget specifications of the T/R chipset are shown in Table 10 below:

Table 10 Specifications of Ku-Band 2W 4-Channel T/R Chipset

TX/Rx	Parameter	Typical Value	Note
TX	Tx Gain	33.5dB	
	Tx Output Power	35.5dBm	
	Tx Power Consumption	10.05W	Single channel
	Tx Efficiency	35.3%	chipset
	Atten. Bits / Step	5bits/0.5dB	
	Atten. Accuracy	≤0.4dB	

	Phase Shift Bits / Step	6bits/5.625°	

	Phase Shift Accuracy（RMS）	⩽3°	
	Phase Shift Spurious AM	±0.8dB	
RX	Rx Gain	28dB	
	Noise figure	⩽2.5dB	
	Rx Input P-1dB	⩾-27dBm	
	Rx Power Consumption	0.26W (1.8V supply) 0.36W (3.3V supply)	Single Channel
	Atten. Bits / Step	6bits/0.5dB	
	Atten. Accuracy	⩽0.4dB	
	Phase Shift Bits / Step	6bits/5.625°	
	Phase Shift Accuracy（RMS）	⩽3°	
	Phase Shift Spurious AM	±0.8dB	

1.5 Ku-Band 5W 4-Channel T/R Chipset Solution

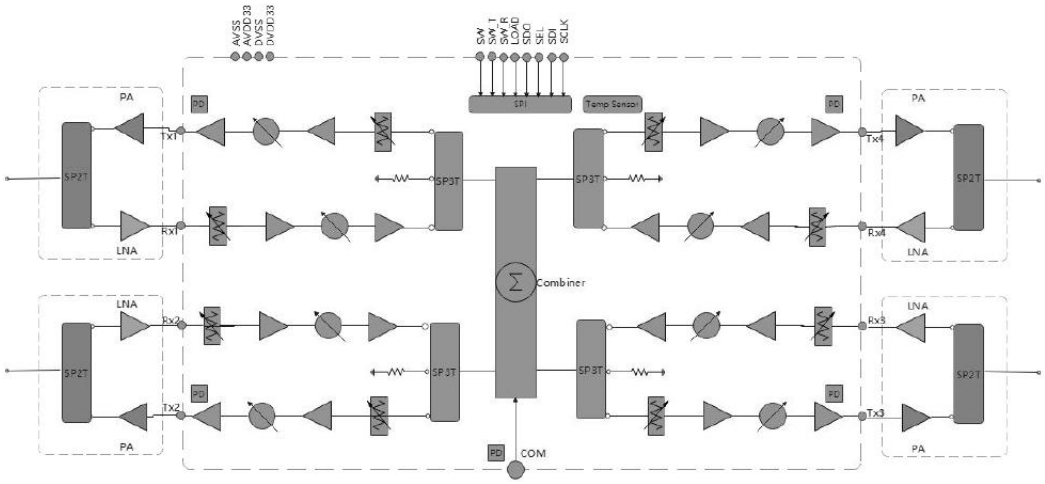

Figure11　Ku-Band 5 W T/R Chipset System Architecture Diagram

1.5.1 Chip Design Solution

The T/R chipset consists of XSC-6520 (4-channel silicon-based amplitude and phase control multifunctional chip), XMF-1218-40 (GaN 10W T/R chip ,derated operation), XDA-0520-21(driver amplifier chip), XLT-1218 (limiter-LNA chip), XPM-28V1A(power supply modulation chip) and XPM-5V1A(power supply modulation chip).

1.5.1.1 Silicon-Based 4-Channel Amplitude-Phase Multi-Function Chip

Refer to 1.1.1.1.

1.5.1.2 200 mW Driver Amp Chip

The driver amplifier adopts GaAs process. Its key specifications are listed as follows:

Table 11 Specifications of XDA-0520-21

Parameter	Typical Value
Operating Frequency	12 GHz ~18.5GHz
Power Gain	17dB
Saturated Output Power	22dBm
Input Return Loss	-12dB
Output Return Loss	-15dB
Power Consumption	5V/140mA
Size	1.27mm*1.27mm*0.1mm

Note: The gain of the driver amplifiert is relatively high. A fixed attenuator shall be connected to the input terminal of the driver amplifier during application to reduce the gain to an appropriate range. The matched driver amplifier is currently under development.

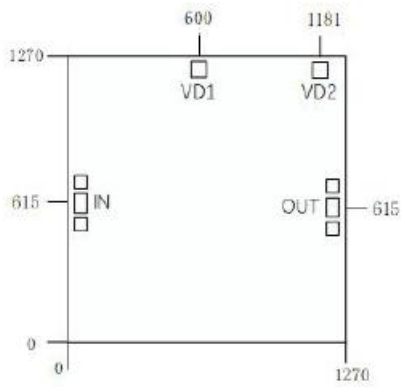

Figure 12 Pad Drawing of XDA-0520-21

Table 12 Pad Assignments for XDA-0520-21

Pad Designation	Function Description	Note
IN	RF input	
OUT	RF Output	
VD1	Drain supply	+5V;
VD2	Drain supply	+5V;

1.5.1.3 XMF-1218-40 PA Switch Chip

- Operating Frequency: 12 GHz~18.5 GHz
- TX Power Gain: ⩾21dB
- Saturated Output Power: ⩾38.5dBm
- PAE: ⩾44.6%
- Power Consumption: ⩽24V/961mA
- Rx Switch Insertion Loss: ⩽1dB
- Switching Time: 20ns
- Switch Control: 0 / -28 V
- Input Return Loss: -10dB
- Output Return Loss: -10dB
- Chip Size: 3.2mm×2mm

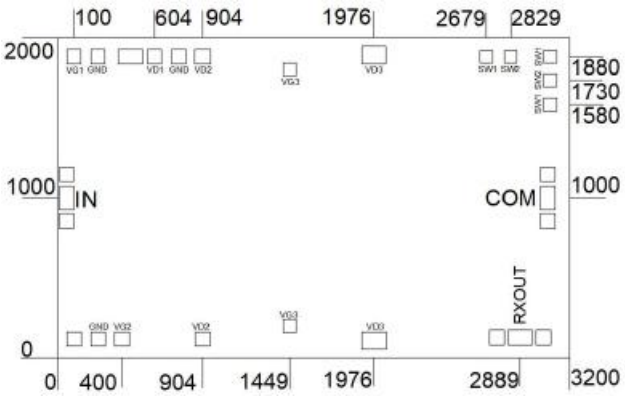

Figure 13 Pad Drawing of XMF-1218-40 PA

Note: PA nominal supply: +28 V, derated to +24 V in practical use.

Table 13 Pad Assignments for XLT-1218(M)

Pad Designation	Function Description	Note
IN	PA Input	
COM	RF Common Port	
RXOUT	Rx Output	
SW1	Switch Ctrl Voltage Port 1	SW1=0V,SW2=-28V, Tx Channel Active; SW1=-28V,SW2=0V, Rx Channel Active;
SW2	Switch Ctrl Voltage Port 2	
Vg1,2,3	Tx PA Gate Supply	-2.4V
VD1,2,3	Tx PA Drain Supply	24V

1.5.1.4 XLT-1218 Limiter-LNA Chip

- Operating Frequency: 12 GHz~18.5 GHz
- Gain: 25dB
- Noise Figure: ≦1.7 dB
- Input P-1: ≥-22dBm
- Power Handling: 10W
- Input Return Loss: -10dB
- Output Return Loss: -10dB
- Power Consumption: 5V/28mA
- Chip Size: 2.3mm×1.2mm

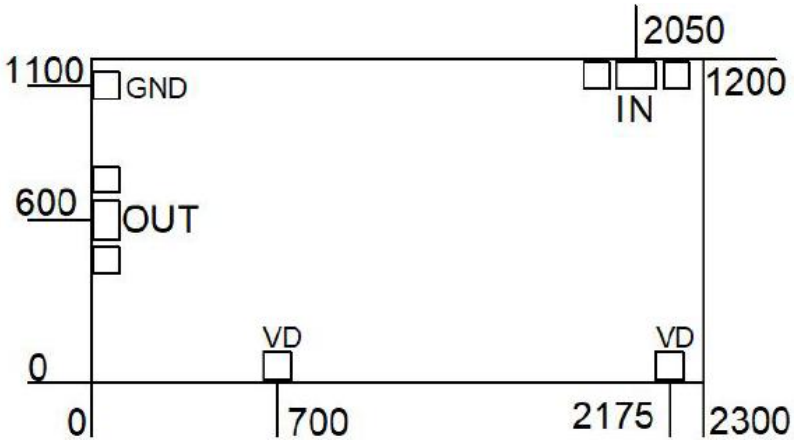

Figure 14 Pad Drawing of XLT-1218

Table 14 Pad Assignments for XLT-1218

Pad Designation	Function Description
IN	RF input
OUT	RF Output
VD	Drain Supply
GND	Gnd PAD

1.5.2 Solution Summary

The solution consists of a four-channel silicon-based multi-functional chip, PA switch chip and limiter-LNA chip. It will use +24V、-28V、+5V、-5V、+3.3V、+1.8V(optional) power supply voltage rails. The overall link budget specifications of the T/R chipset are shown in Table 10 below:

Table 15 Specifications of Ku-Band 5W 4-Channel T/R Chipset

TX/Rx	Parameter	Typical Value	Note
TX	Tx Gain	38.5dB	
	Tx Output Power	38.5dBm	chipset
	Tx Power Consumption	27.6W	Single channel
	Tx Efficiency	29.4%	chipset
	Atten. Bits / Step	5bits/0.5dB	
	Atten. Accuracy	≤0.5dB	
	Phase Shift Bits / Step	6bits/5.625°	
	Phase Shift Accuracy（RMS）	≤3°	
	Phase Shift Spurious AM	±1dB	
RX	Rx Gain	28dB	1
	Noise figure	≤3.4dB	

	Rx Input P-1dB	⩾-27dBm	
	Rx Power Consumption	0.26W (1.8V supply) 0.36W (3.3V supply)	Single Channel
	Atten. Bits / Step	6bits/0.5dB	
	Atten. Accuracy	⩽0.4dB	
	Phase Shift Bits / Step	6bits/5.625°	
	Phase Shift Accuracy（RMS）	⩽3°	
	Phase Shift Spurious AM	±1dB	

1.6 Ku-Band 10W 4-Channel T/R Chipset Solution

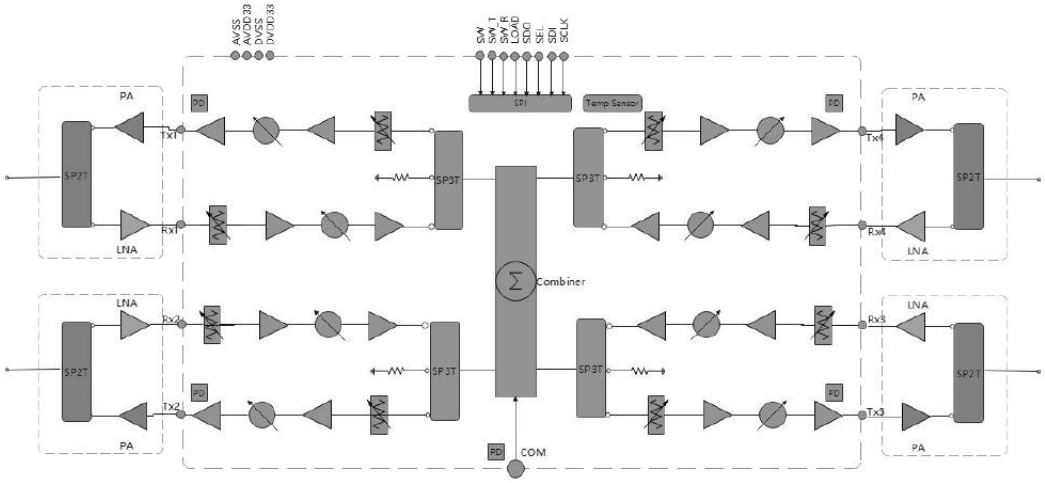

Figure15 Ku-Band 10 W T/R Chipset System Architecture Diagram

1.6.1 Chip Design Solution

Refer to 1.1.1.1.

1.6.1.1 200 mW Driver Amp Chip

The driver amplifier adopts GaAs process. Its key specifications are listed as follows:

Table 16 Specifications of Driver amplifier

Parameter	Typical Value
Operating Frequency	12 GHz ~18.5GHz

Power Gain	9.5dB
Saturated Output Power	22dBm
Input Return Loss	-12dB
Output Return Loss	-15dB
Power Consumption	5V/140mA
Size	1.27mm*1.27mm*0.1mm

Note: The gain of the driver amplifiert is relatively high. A fixed attenuator shall be connected to the input terminal of the driver amplifier during application to reduce the gain to an appropriate range. The matched driver amplifier is currently under development.

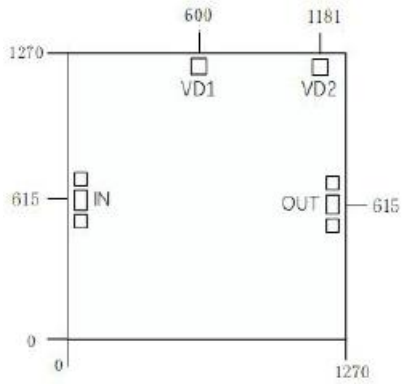

Figure 16 Pad Drawing of Driver amplifier

Table 17 Pad Assignments for Driver amplifier

Pad Designation	Function Description	Note
IN	RF input	
OUT	RF Output	
VD1	Drain supply	+5V;
VD2	Drain supply	+5V;

1.6.1.2 GaN PA Switch Chip

- Operating Frequency: 12 GHz~18.5 GHz
- TX Power Gain: ≥21dB
- Saturated Output Power: ≥40.7dBm

- PAE: ⩾41%
- Power Consumption: ⩽28V/1150mA
- Rx Switch Insertion Loss: ⩽1dB
- Switching Time: 20ns
- Switch Control: 0 / -28 V
- Input Return Loss: -15dB
- Output Return Loss: -15dB
- Chip Size: 3.2mm×2mm×0.08mm

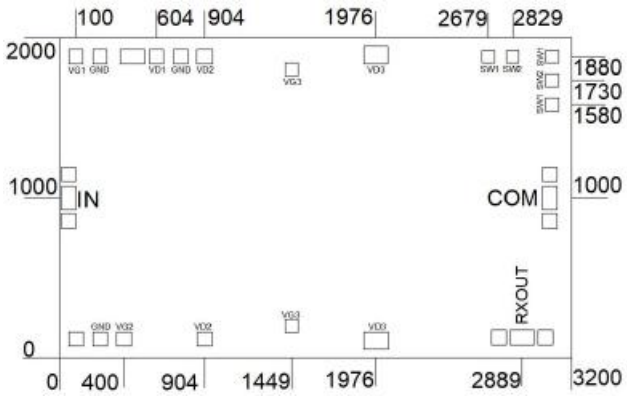

Figure 17 Pad Drawing of Driver amplifier

Table 18 Pad Assignments for XLT-1218(M)

Pad Designation	Function Description	Note
IN	PA Input	
COM	RF Common Port	
RXOUT	Rx Output	
SW1	Switch Ctrl Voltage Port 1	SW1=0V,SW2=-28V, Tx Channel Active; SW1=-28V,SW2=0V, Rx Channel Active;
SW2	Switch Ctrl Voltage Port 2	
Vg1,2,3	Tx PA Gate Supply	
VD1,2,3	Tx PA Drain Supply	28V

1.6.1.3 GaAs Limiter-LNA Chip

- Operating Frequency: 12 GHz~18.5 GHz
- Gain: 25dB
- Noise Figure: ⩽1.7 dB

- Input P-1: ⩾-22dBm
- Power Handling: 10W
- Input Return Loss: -10dB
- Output Return Loss: -10dB
- Power Consumption: 5V/28mA
- Chip Size: 2.3mm×1.2mm

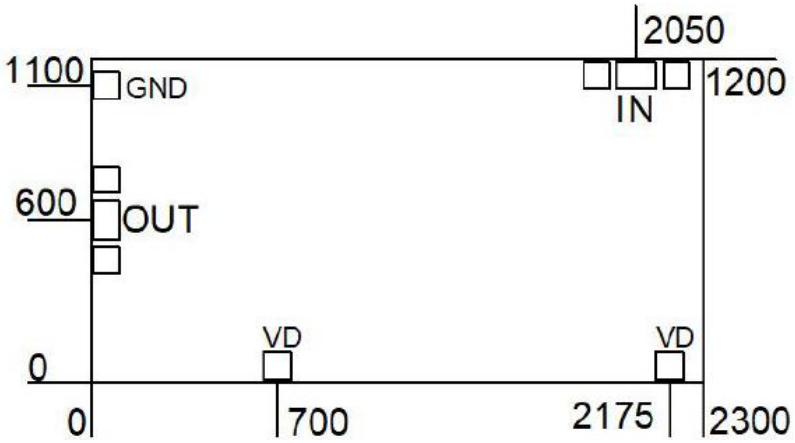

Figure 18 Pad Drawing of XLT-1218

Table 19 Pad Assignments for XLT-1218

Pad Designation	Function Description
IN	RF input
OUT	RF Output
VD	Drain Supply
GND	Gnd PAD

1.6.2 Solution Summary

The solution consists of a four-channel silicon-based multi-functional chip, PA switch chip and limiter-LNA chip. It will use +28V、-28V、+5V、-5V、+3.3V、+1.8V(optional) power supply voltage rails. The overall link budget specifications of the T/R chipset are shown in Table 10 below:

Table 20 Specifications of Ku-Band 5W 4-Channel T/R Chipse

TX/Rx	Parameter	Typical Value	Note
	Tx Gain	39.5dB	

TX	Tx Output Power	40.7dBm	chipset
	Tx Power Consumption	33.4W	Single channel
	Tx Efficiency	37%	chipset
	Atten. Bits / Step	5bits/0.5dB	
	Atten. Accuracy	≤0.4dB	
	Phase Shift Bits / Step	6bits/5.625°	
	Phase Shift Accuracy（RMS）	≤3°	
	Phase Shift Spurious AM	±0.8dB	
RX	Rx Gain	28dB	1
	Noise figure	≤3.1dB	
	Rx Input P-1dB	≥-27dBm	
	Rx Power Consumption	0.36W	Single Channel
	Atten. Bits / Step	6bits/0.5dB	
	Atten. Accuracy	≤0.4dB	
	Phase Shift Bits / Step	6bits/5.625°	
	Phase Shift Accuracy（RMS）	≤3°	
	Phase Shift Spurious AM	±0.8dB	

2. Ka-Band Chipset Solution

2.1 Ka-Band 0.5W 4-Channel T/R Chipset Solution

2.1.1 Chip Design Solution

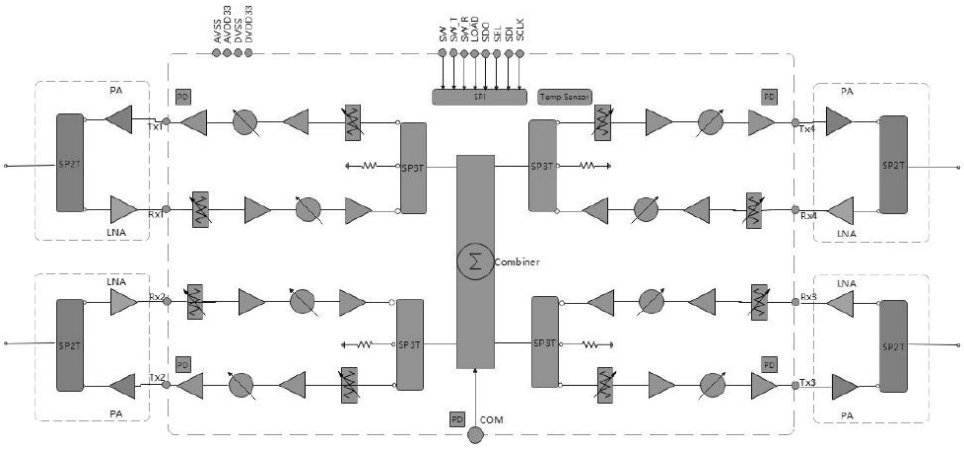

Figure 1 Ka-Band 0.5 W T/R Chipset System Architecture Diagram

To meet the application requirements of Ka-band 4-channel T/R modules, a T/R chipset solution composed of the 4-channel silicon-based amplitude-phase control multifunctional chip XSC-6721 and 0.5 W GaAs transceiver multifunctional chip is proposed.Each channel of the 4-channel silicon-based amplitude-phase control multifunctional chip integrates an internal phase shifter, attenuator, low-noise amplifier, driver amplifier, transmit-receive switching interface and other circuits. The phase shifter and attenuator perform phase shifting and attenuation functions, while the RF switch realizes receiving and transmitting switching. The enable signal is generated internally by the multifunctional chip XSC-6721, eliminating the need for an external power supply modulation chip. This design not only reduces costs but also simplifies the complexity of the module.

2.1.1.1 Silicon-Based 4-Channel Amplitude-Phase Multi-Function Chip

- Operating Frequency: 32 GHz~38 GHz
- Rx Gain: ⩾1 dB

  Note: including 1-to-4 power division loss.
- Tx Gain: ⩾6 dB

  Note: including 1-to-4 power division loss.
- Rx Input P-1: ⩾-8 dBm
- Tx Output P-1: ⩾11 dBm
- Noise figure: ⩽14dB
- Phase Shift Resolution: 6 bits
- Phase Shift Step: 5.625°
- Phase Shift Error (RMS): 3°
- Phase Shift Amplitude Variation: 1.5 dB
- Attenuation Bits: 4bits(TX), 6bits(RX)
- Attenuation Step: 0.5dB
- Attenuation Error (RMS): 0.5dB(TX), 0.3dB(RX)
- Attenuation Phase Variation: 7°

- Operating Voltage: Digital/Analog, 3.3 V; RF, 3.3 V or 1.8 V (selectable)
- RX Quiescent Current: 65 mA/Chanel
- Tx Dynamic Current: 100 mA /Chanel
- Chip Dimensions: 3 mm × 6 mm × 0.2 mm
- Pad Layout: As shown in Figure 20

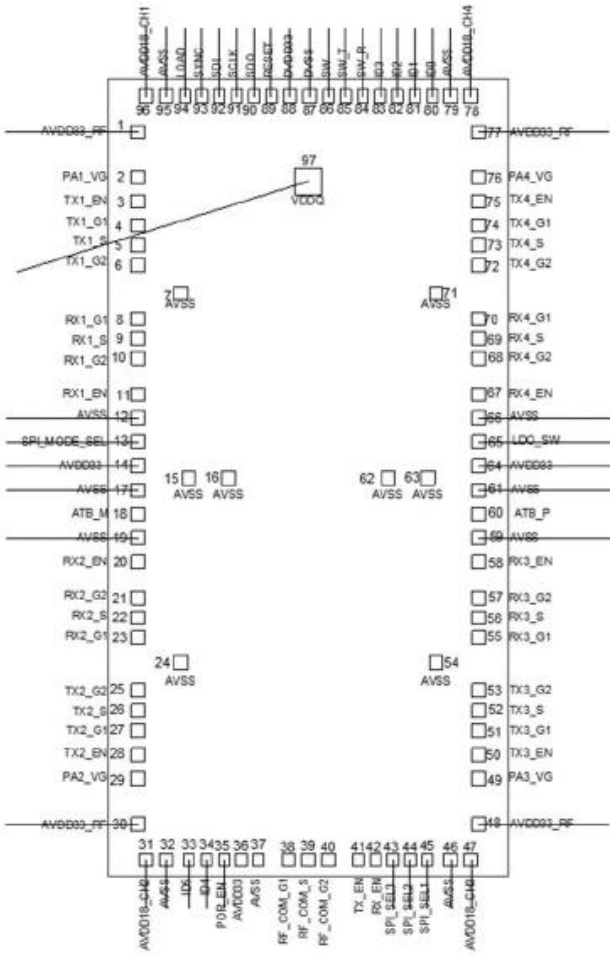

Figure 2 Pad Layout of Ka 4-Channel Amplitude-Phase Multi-Function Chip

The size of RF GSG pads is 100 μm × 100 μm with a pitch of 150 μm, and the typical chip thickness is 200 μm. The port layout of XSC-6721 is shown in the figure; the numerals denote pad numbers ranging from 1 to 97, and the lower-left corner serves as the reference origin.

Table 1 Pad Definition of Amplitude-Phase Multi-Function Chip

No	Name	X axis	Y axis	PAD size (um)	Type	Description	level	Notes
1	AVDD33_RF	220.0	5603.0	100x100	POWER	RF 3.3V Supply		
						External PA Gate Bias Voltage for		

2	PA1_VG	220.0	5303.0	100x100	OUTPUT	CH1		
3	TX1_EN	220.0	5123.0	100x100	OUTPUT	TX Enable, CH1	H	
4	TX1_G1	220.0	4900.0	100x100	GND	RF GND		
5	TX1_S	220.0	4750.0	100x100	OUTPUT	RF Output, CH1		
6	TX1_G2	220.0	4600.0	100x100	GND	RF GND		
7	AVSS	540.0	4386.0	100x101	GND	RF GND		
8	RX1_G1	220.0	4200.0	100x100	GND	RF GND		
9	RX1_S	220.0	4050.0	100x100	INPUT	RF Input, CH1		
10	RX1_G2	220.0	3900.0	100x100	GND	RF GND		
11	RX1_EN	220.0	3630.0	100x100	OUTPUT	RX Enable, CH1	H	
12	AVSS	220.0	3450.0	100x100	GND	RF GND		
13	SPI_MODE_SEL	220.0	3270.0	100x100	INPUT	SPI Mode Selection: Low level for 4-wire mode, high level for 3-wire mode		
14	AVDD33	220.0	3090.0	100x100	POWER	Analog 3.3V Supply		
15	AVSS	602.0	3000.0	100x100	GND	RF GND		
16	AVSS	902.0	3000.0	100x100	GND	RF GND		
17	AVSS	220.0	2910.0	100x100	GND	Analog GND		
18	ATB_M	220.0	2730.0	100x100	OUTPUT	Internal Node Test Port _M		
19	AVSS	220.0	2550.0	100x100	GND	RF GND		
20	RX2_EN	220.0	2370.0	100x100	OUTPUT	RX Enable, CH2		
21	RX2_G2	220.0	2100.0	100x100	GND	RF GND		
22	RX2_S	220.0	1950.0	100x100	INPUT	RF Input, CH2		

23	RX2_G1	220.0	1800.0	100x100	GND	RF GND		
24	AVSS	540.0	1614.0	100x100	GND	RF GND		
25	TX2_G2	220.0	1400.0	100x100	GND	RF GND		
26	TX2_S	220.0	1250.0	100x100	OUTPUT	RF Output, CH2		
27	TX2_G1	220.0	1100.0	100x100	GND	RF GND		
28	TX2_EN	220.0	877.0	100x100	OUTPUT	TX Enable, CH2	H	
29	PA2_VG	220.0	697.0	100x100	OUTPUT	External PA Gate Bias Voltage for CH2		
30	AVDD33_RF	220.0	397.0	100x100	POWER	RF 3.3V Supply		
31	AVDD18_CH2	280.0	130.0	100x100	POWER	RF 1.8V Supply		
32	AVSS	430.0	130.0	100x100	GND	RF GND		
33	ID5（AVSS）	605.0	130.0	80x100	INPUT	ID Bit		Default: Low
34	ID4（AVSS）	735.0	130.0	80x100	INPUT	ID Bit		Default: Low
35	POR_EN	865.0	130.0	80x100	INPUT	Power-on Reset Enable		
36	AVDD33	995.0	130.0	80x100	POWER	Analog 3.3V Supply		
37	AVSS	1125.0	130.0	80x100	GND	Analog GND		
38	RF_COM_G1	1350.0	130.0	100x100	GND	RF GND		
39	RF_COM_S	1500.0	130.0	100x100	IN/OUTPUT	Common RF Port		
40	RF_COM_G2	1650.0	130.0	100x100	GND	RF GND		
41	TX_EN	1875.0	130.0	80x100	OUTPUT	TX enable flag	H	“Or” of TX*_EN
42	RX_EN	2005.0	130.0	80x100	OUTPUT	RX enable flag	H	“Or” of RX*_EN
43	SPI_SEL3	2135.0	130.0	80x100	INPUT	Protocol Selection		
44	SPI_SEL2	2265.0	130.0	80x100	INPUT	Protocol Selection		

45	SPI_SEL1	2395.0	130.0	80x100	INPUT	Protocol Selection		
46	AVSS	2570.0	130.0	100x100	GND	RF GND		
47	AVDD18_CH3	2720.0	130.0	100x100	POWER	RF 1.8V Supply		
48	AVDD33_RF	2780.0	397.0	100x100	POWER	RF 3.3V Supply		
49	PA3_VG	2780.0	697.0	100x100	OUTPUT	External PA Gate Bias Voltage for CH3		
50	TX3_EN	2780.0	877.0	100x100	OUTPUT	TX Enable, CH3	H	
51	TX3_G1	2780.0	1100.0	100x100	GND	RF GND		
52	TX3_S	2780.0	1250.0	100x100	OUTPUT	RF Output, CH3		
53	TX3_G2	2780.0	1400.0	100x100	GND	RF GND		
54	AVSS	2460.0	1614.0	100x100	GND	RF GND		
55	RX3_G1	2780.0	1800.0	100x100	GND	RF GND		
56	RX3_S	2780.0	1950.0	100x100	INPUT	RF Input, CH3		
57	RX3_G2	2780.0	2100.0	100x100	GND	RF GND		
58	RX3_EN	2780.0	2370.0	100x100	OUTPUT	RX Enable, CH3	H	
59	AVSS	2780.0	2550.0	100x100	GND	RF GND		
60	ATB_P	2780.0	2730.0	100x100	OUTPUT	Internal Node Test Port _P		
61	AVSS	2780.0	2910.0	100x100	GND	Analog GND		
62	AVSS	2398.0	3000.0	100x100	GND	RF GND		
63	AVSS	2098.0	3000.0	100x100	GND	RF GND		
64	AVDD33	2780.0	3090.0	100x100	POWER	Analog 3.3V Supply		
65	LDO_SW	2780.0	3270.0	100x100	INPUT	LDO Switch		Default to low
66	AVSS	2780.0	3450.0	100x100	GND	RF GND		
67	RX4_EN	2780.0	3630.0	100x100	OUTPUT	RX Enable, CH4	H	

68	RX4_G2	2780.0	3900.0	100x100	GND	RF GND		
69	RX4_S	2780.0	4050.0	100x100	INPUT	RF Input, CH4		
70	RX4_G1	2780.0	4200.0	100x100	GND	RF GND		
71	AVSS	2460.0	4386.0	100x100	GND	RF GND		
72	TX4_G2	2780.0	4600.0	100x100	GND	RF GND		
73	TX4_S	2780.0	4750.0	100x100	OUTPUT	RF Output, CH4		
74	TX4_G1	2780.0	4900.0	100x100	GND	RF GND		
75	TX4_EN	2780.0	5123.0	100x100	OUTPUT	TX Enable, CH4	H	
76	PA4_VG	2780.0	5303.0	100x100	OUTPUT	External PA Gate Bias Voltage for CH4		
77	AVDD33_RF	2780.0	5603.0	100x100	POWER	RF 3.3V Supply		
78	AVDD18_CH4	2720.0	5870.0	100x100	POWER	RF 1.8V Supply		
79	AVSS	2570.0	5870.0	100x100	GND	RF GND		
80	ID0(SDO/DVSS)	2430.0	5870.0	80x100	INPUT	ID Bit		Default pull-up
81	ID1(OD_EN/SYN)	2300.0	5870.0	80x100	INPUT	ID Bit		Default to low
82	ID2(OE/MODE)	2170.0	5870.0	80x100	INPUT	ID Bit		Default to low
83	ID3(RM/DVSS)	2040.0	5870.0	80x100	INPUT	ID Bit		Default to low
84	SW_R	1910.0	5870.0	80x100	INPUT	T/R Switch, SW_R		Default to low
85	SW_T	1780.0	5870.0	80x100	INPUT	T/R Switch, SW_T		Default to low
86	SW	1650.0	5870.0	80x100	INPUT	T/R Switch, SW		Default to low
87	DVSS	1510.0	5870.0	100x100	GND	Digital GND		
88	DVDD33	1360.0	5870.0	100x100	POWER	Digital 3.3V Supply		
89	RESET	1220.0	5870.0	80x100	INPUT	Reset Signal		
90	SDO	1090.0	5870.0	80x100	OUTPUT	Serial Data Output	L	

91	SCLK	960.0	5870.0	80x100	INPUT	Serial Clock		
92	SDI	830.0	5870.0	80x100	IN/OUTPUT	Serial Data Input		
93	SYNC	700.0	5870.0	80x100	INPUT	Chip Select signal, active low		
94	LOAD	570.0	5870.0	80x100	INPUT	Latch signal, rising edge triggered		
95	AVSS	430.0	5870.0	100x100	GND	RF GND		
96	AVDD18_CH1	280.0	5870.0	100x100	POWER	RF 1.8V Supply		
97	VDDQ	1500.0	5181.0	200x200	POWER	eFuse 2.5V Supply		

2.1.1.2 GaAs Transceiver Multi-chip (Mirror Version Available)

- Operating Frequency: 32 GHz~38 GHz
- TX Power Gain: ⩾19dB
- Saturated Output Power: ⩾28dBm
- PAE: ⩾25%
- RX Gain: 25dB
- Rx Input P-1: -21 dBm
- Noise Figure: 3.3 dB
- RX Quiescent Power Consumption: +3.3 V / 29 mA (Typical)
- Chip Size: 1.9mm×2.19mm×0.10mm

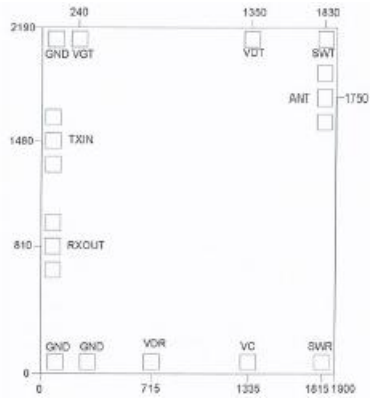

Figure 3 GaAs Multifunction T/R Chip Pad Layout

Table 2 GaAs Multifunction T/R Chip Pad Assignments

Pad Designation	Function Description
VGT	External TX Amplifier Gate Bias Voltage (-0.55V)
VDT	External TX Amplifier Drain Bias Voltage(5V)
VDR	External RX Amplifier Gate Bias Voltage (3.3V)
SWT	Switch Control Pad, SWT
SWR	Switch Control Pad, SWR
TX_IN	TX Input RF Port
RX_OUT	RX Output RF Port
ANT	Common RF Port
VC	Limiter Control Pad

2.1.2 Solution Summary

The overall link budget specifications of the T/R chipset are shown in Table 13 below:

Table 3 Specifications of Ku-Band 0.5W 4-Channel T/R Chipset

TX or RX	Parameter	Typical Value	Note
TX	Tx Gain	25dB	Power Gain
	Tx Output Power	28dBm	
	Tx Power Consumption	2.33W	
	Tx Efficiency	22%	
	Atten. Bits / Step	4bits/0.5dB	
	Atten. Accuracy	0.5dB	
	Phase Shift Bits / Step	6bits/5.625°	
	Phase Shift Accuracy（RMS）	3°	
	Phase Shift Spurious AM	±0.75dB	

RX	Rx Gain	25dB	
	Noise figure	4dB	
	Rx Input P-1dB	-21dBm	
	Rx Power Consumption	0.19W	Low Power Mode
	Atten. Bits / Step	6bits/0.5dB	Maximum Attenuation: 23.5 dB
	Atten. Accuracy	0.5dB	
	Phase Shift Bits / Step	6bits/5.625°	
	Phase Shift Accuracy（RMS）	3°	
	Phase Shift Spurious AM	±0.75dB	